AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A nonvolatile memory with spacer trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a control gate structure formed on said gate oxide;

a spacer trapping structure including a first isolation layer formed over the sidewall of said control gate structure;~~first spacers~~ and a dielectric spacer formed on the ~~sidewall of~~ said first isolation layer, wherein said ~~first spacers~~ spacer trapping structure includes charge trapping capability thereby storing single or multiple bits of data;

source and drain regions formed adjacent to said control gate structure, wherein p-n junctions of said source and drain regions formed under said ~~first spacers~~ spacer trapping structure; and

silicide ~~optionally~~ formed on said control gate structure and said source and drain regions.

2. (Currently Amended) The nonvolatile memory of Claim 1, further comprising pocket ion implantation region located adjacent to said source and drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the p-n junctions of said pocket ion implantation region formed under said ~~first spacers~~spacer trapping structure.

3. (Currently Amended) The nonvolatile memory of Claim 1, further comprising:

lightly doped drain region adjacent to said source and drain regions, wherein p-n junctions of said lightly doped drain regions formed under said ~~first spacers~~spacer trapping structure and the p-n junction of said lightly doped

drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

4. (Currently Amended) The nonvolatile memory of Claim 1, further comprising:

double doped drain region adjacent to said source and drain regions, wherein p-n junctions of said double doped drain regions formed under said ~~first spacers~~spacer trapping structure and the p-n junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions and the doping concentration of said double doped drain region is lower than the one of said source and drain regions; and

pocket ion implantation region adjacent to said double doped drain region, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

5. (Currently Amended) The nonvolatile memory of Claim 1, wherein said spacer trapping structure further comprises a second isolation layer formed between said first isolation layer and said ~~first spacer~~dielectric spacer, said second isolation layer being formed of nitride or the material having energy gap lower than 6eV, ~~wherein~~ said first isolation layer ~~includes~~ including oxide or the material having energy gap greater than 7eV, said ~~first spacers~~dielectric spacer attached onto the sidewall of said second isolation layer are formed of oxide or the material having energy gap larger than 7eV.

6. (Currently Amended) The nonvolatile memory of Claim 2, wherein said spacer trapping structure further comprises a second isolation layer formed between said first isolation layer and said ~~first spacer~~dielectric spacer, said second isolation layer being formed of nitride or the material having energy gap lower than 6eV, wherein said first isolation layer ~~includes~~including oxide or the material having energy gap greater than 7eV, said ~~first spacers~~dielectric spacer attached onto the sidewall of said second isolation layer are formed of oxide or the material having energy gap larger than 7eV.

7. (Currently Amended) The nonvolatile memory of Claim 3, wherein said spacer trapping structure further comprises a second isolation layer formed between said first isolation layer and said ~~first spacer~~dielectric spacer, said second isolation layer being formed of nitride or the material having energy gap lower than 6eV, wherein said first isolation layer includes oxide or the material having energy gap greater than 7eV, said ~~first spacers~~dielectric spacer attached onto the sidewall of said second isolation layer are formed of oxide or the material having energy gap larger than 7eV.

8. (Currently Amended) The nonvolatile memory of Claim 4, wherein said spacer structure further comprises a second isolation layer formed between said first isolation layer and said ~~first spacer~~dielectric spacer, said second isolation layer being formed of nitride or the material having energy gap lower than 6eV, wherein said first isolation layer ~~includes~~including oxide or the material having energy gap greater than 7eV, said ~~first spacers~~dielectric attached onto the sidewall of said second isolation layer are formed of oxide or the material having energy gap larger than 7eV.

9. (Original) The nonvolatile memory of Claim 5, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4eV.

10. (Original) The nonvolatile memory of Claim 6, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4eV.

11. (Original) The nonvolatile memory of Claim 7, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4eV.

12. (Original) The nonvolatile memory of Claim 8, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4eV.

13. (Original) The nonvolatile memory of Claim 1, wherein said first isolation layer is formed of oxide or the material having energy gap larger than 7eV.

14. (Currently Amended) The nonvolatile memory of Claim 1, wherein said ~~first spacers are~~dielectric spacer is formed of nitride or the material having energy gap lower than 6eV.

15. (Original) The nonvolatile memory of Claim 1, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

16. (Original) The nonvolatile memory of Claim 2, wherein said first isolation layer is formed of oxide or the material having energy gap larger than 7eV.

17. (Currently Amended) The nonvolatile memory of Claim 2, wherein said ~~first spacers are~~dielectric spacer is formed of nitride or the material having energy gap lower than 6eV.

18. (Original) The nonvolatile memory of Claim 2, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

19. (Original) The nonvolatile memory of Claim 3, wherein said first isolation layer is formed of oxide or the material having energy gap larger than 7eV.

20. (Currently Amended) The nonvolatile memory of Claim 3, wherein said ~~first spacers are~~dielectric spacer is formed of nitride or the material having energy gap lower than 6eV.

21. (Original) The nonvolatile memory of Claim 3, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

22. (Original) The nonvolatile memory of Claim 4, wherein said first isolation layer is formed of oxide or the material having energy gap larger than 7eV.

23. (Currently Amended) The nonvolatile memory of Claim 4, wherein said ~~first spacers are~~dielectric spacer is formed of nitride or the material having energy gap lower than 6eV.

24. (Original) The nonvolatile memory of Claim 4, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

25. (Previously Presented) A nonvolatile memory with spacertrapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a control gate structure formed on said gate oxide, wherein said control gate structure comprises a stacked structure including of polysilicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed on the sidewall of said control gate structure and the surface of said semiconductor substrate;

first spacers formed on the sidewall of said second dielectric layer, wherein said first spacers include charge trapping capability thereby storing single or multiple bits of data; and

source and drain regions formed adjacent to said gate structure, wherein p-n junctions of said source and drain regions formed under said first spacers.

26. (Original) The nonvolatile memory of Claim 25, further comprising pocket ion implantation region located adjacent to said source and drain regions, wherein the p-n junctions of said pocket ion implantation region formed under said first spacers, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

27. (Original) The nonvolatile memory of Claim 25, further comprising:

lightly doped drain region adjacent to said source and drain regions, wherein the p-n junctions of said lightly doped drain formed under said first spacers, the junction of said lightly doped drain region being shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

28. (Original) The nonvolatile memory of Claim 25, further comprising:

double doped drain region adjacent to said source and drain regions, wherein the p-n junctions of said double doped drain region are formed under said first spacers and the junction of said double doped drain region being deeper than the one of said source and drain regions, said double doped drain region being closer to the channel under said gate structure than said source and drain regions and the doping concentration of said double doped drain region is lower than the one of said source and drain regions; and

pocket ion implantation region adjacent to said double doped drain region, the conductive type of the pocket ion implantation region being opposite to the one of the source and drain regions.

29. (Original) The nonvolatile memory of Claim 25, further comprises a third dielectric layer formed between said second dielectric layer and said first spacer, said third dielectric layer being formed of nitride or the material having energy gap lower than 6eV, wherein said second dielectric layer includes oxide or the material having energy gap greater than 7eV, said first spacers attached onto the sidewall of said third dielectric layer are formed of oxide or the material having energy gap larger than 7eV.

30. (Original) The nonvolatile memory of Claim 26, further comprises a third dielectric layer formed between said second dielectric layer and said first spacer, said third dielectric layer being formed of nitride or the material having energy gap lower than 6eV, wherein said second dielectric layer includes oxide or the material having energy gap greater than 7eV, said first spacers attached onto the sidewall of said third dielectric layer are formed of oxide or the material having energy gap larger than 7eV.

31. (Original) The nonvolatile memory of Claim 27, further comprises a third dielectric layer formed between said second dielectric layer and said first spacer, said third dielectric layer being formed of nitride or the material having energy gap lower than 6eV,

wherein said second dielectric layer includes oxide or the material having energy gap greater than 7eV, said first spacers attached onto the sidewall of said third dielectric layer are formed of oxide or the material having energy gap larger than 7eV.

32. (Original) The nonvolatile memory of Claim 28, further comprises a third dielectric layer formed between said second dielectric layer and said first spacer, said third dielectric layer being formed of nitride or the material having energy gap lower than 6eV, wherein said second dielectric layer includes oxide or the material having energy gap greater than 7eV, said first spacers attached onto the sidewall of said third dielectric layer are formed of oxide or the material having energy gap larger than 7eV.

33. (Original) The nonvolatile memory of Claim 29, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4 eV.

34. (Original) The nonvolatile memory of Claim 30, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4 eV.

35. (Original) The nonvolatile memory of Claim 31, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4 eV.

36. (Original) The nonvolatile memory of Claim 32, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide, nitride or the material having energy gap greater than 4 eV.

37. (Original) The nonvolatile memory of Claim 25, wherein said second dielectric layer is formed of oxide or the material having energy gap greater than 7eV.

38. (Original) The nonvolatile memory of Claim 25, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

39. (Original) The nonvolatile memory of Claim 25, wherein said silicide material includes $TiSi_2$, WSi_2.

40. (Original) The nonvolatile memory of Claim 25, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

41. (Original) The nonvolatile memory of Claim 26, wherein said second dielectric layer is formed of oxide or the material having energy gap grater than 7eV.

42. (Original) The nonvolatile memory of Claim 26, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

43. (Original) The nonvolatile memory of Claim 26, wherein said silicide material includes $TiSi_2$, WSi_2.

44. (Original) The nonvolatile memory of Claim 26, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

45. (Currently Amended) The nonvolatile memory of Claim 27, wherein said second dielectric layer is formed of oxide or the material having energy gap greater than 7eV.

46. (Original) The nonvolatile memory of Claim 27, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

47. (Original) The nonvolatile memory of Claim 27, wherein said silicide material includes $TiSi_2$, WSi_2.

48. (Original) The nonvolatile memory of Claim 27, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

49. (Original) The nonvolatile memory of Claim 28, wherein said wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

50. (Original) The nonvolatile memory of Claim 28, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

51. (Original) The nonvolatile memory of Claim 28, wherein said silicide material includes $TiSi_2$, WSi_2.

52. (Previously Presented) The nonvolatile memory of Claim 28, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.